Assignee: Intel Corporation

CLAIMS

What is claimed is:

1   1.   An apparatus, comprising:
2   a trace cache array to store a first trace and a second trace; and
3   a trace-end predictor to store a first tail data from said first trace
4 to predict an address for said second trace.

1   2.   The apparatus of claim 1, wherein said first tail data
2 includes a set and a way for a head of said second trace.

1   3.   The apparatus of claim 1, wherein said first tail data
2 includes a quickstew.

1   4.   The apparatus of claim 1, wherein said trace end predictor
2 is to read said first tail data when a first tail of said first trace is
3 accessed.

1   5.   The apparatus of claim 1, wherein said trace end predictor
2 is to read said first tail data when a first body before a first tail of said
3 first trace is accessed.

1   6.   The apparatus of claim 1, further comprising a selector to
2 select said address from said trace-end predictor and a predictor.

1   7.   The apparatus of claim 6, wherein said selector to give
2 priority to said predictor.

1   8.   The apparatus of claim 1, wherein said trace-end predictor
2 to store a third tail data from a third trace to predict an address for a
3 fourth trace.

1   9.   The apparatus of claim 8, wherein said trace-end predictor
2 is to store tag data of said first trace and said third trace to determine
3 which trace is currently in execution.

1   10.   A method, comprising:
2   storing tail data of a first trace during a first execution of said
3 first trace;
4   retrieving said tail data during a second execution of said first
5 trace; and
6   fetching a head of a second trace from a trace cache using said
7 tail data.

1   11.   The method of claim 10, wherein said storing includes
2 storing set and way information of said first trace.

1   12.   The method of claim 10, wherein said storing includes
2 storing set and way information of said head.

1   13.   The method of claim 10, wherein said storing includes
2 storing a quickstew.

1   14.   The method of claim 13, further comprising calculating a
2 headstew for said second trace using said quickstew.

1   15.   The method of claim 10, wherein said retrieving is
2 performed subsequent to initiating access to a tail of said first trace
3 during said second execution.

1   16.   The method of claim 10, wherein said retrieving is
2 performed subsequent to initiating access to a body of said first trace
3 prior to a tail of said first trace during second execution.

1   17.   The method of claim 10, further comprising inhibiting said
2 fetching when an off-trace prediction is made.

1   18.   An apparatus, comprising:
2   means for storing tail data of a first trace during a first execution
3 of said first trace;
4   means for retrieving said tail data during a second execution of
5 said first trace; and
6   means for fetching a head of a second trace from a trace cache
7 using said tail data.

1   19.   The apparatus of claim 18, wherein said means for storing
2 includes means for storing set and way information of said first trace.

1   20.   The apparatus of claim 18, wherein said means for storing
2 includes means for storing set and way information of said head.

1   21.   The apparatus of claim 18, wherein said means for storing
2 includes means for storing a quickstew.

1   22.   The apparatus of claim 21, further comprising means for
2 calculating a headstew for said second trace using said quickstew.

1   23.   A system, comprising:
2   a processor including a trace cache array to store a first trace and
3 a second trace, and a trace-end predictor to store a first tail data from
4 said first trace to predict an address for said second trace;
5   a memory coupled to said processor to store instructions to be
6 decoded to supply said trace cache array; and
7   an audio input/output device coupled to said memory and to said
8 processor.

1   24.   The system of claim 23, wherein said first tail data includes
2   a set and a way for a head of said second trace.

1   25.   The system of claim 23, wherein said first tail data includes
2   a quickstew.

1   26.   The system of claim 23, wherein said trace end predictor is
2   to read said first tail data when a first tail of said first trace is accessed.

1   27.   The system of claim 23, wherein said trace end predictor is
2   to read said first tail data when a first body before a first tail of said first
3   trace is accessed.